Avnet PicoZed 7015/7030
Pin Changes, Rev B to Rev C

The following changes were made to better align clock-capable pins on the MicroHeaders with the PicoZed 7010/7020 version. Clock capable pins are shown in bold.

17 Dec 2014 -- Initial release
31 Mar 2015 -- Correction on BANK13_LVDS_2_P/N

Affected Signals	MicroHeader Pins	Connected To Rev B U1 @	Moved to Rev C U1 @	New Rev C U1 Pin Name
JX1 (Bank 35 and some Bank 13)				
JX1_LVDS_7_P/N	30,32	D3/C3	B2/B1	IO_L18_T2_AD13_35
JX1_LVDS_10_P/N	41,43	D1/C1	**C6/C5**	**IO_L11_SRCC_35**
JX1_LVDS_11_P/N	42,44	B2/B1	**D5/C4**	**IO_L12_MRCC_35**
JX1_LVDS_12_P/N	47,49	E2/D2	**B4/B3**	**IO_L13_MRCC_35**
JX1_LVDS_13_P/N	48,50	A2/A1	**D3/C3**	**IO_L14_SRCC_35**
JX1_LVDS_14_P/N	53,55	D5/C4	D1/C1	IO_L16_T2_35
JX1_LVDS_15_P/N	54,56	C6/C5	A2/A1	IO_L15_T2_DQS_AD12_35
JX1_LVDS_16_P/N	61,63	B4/B3	E2/D2	IO_L17_T2_AD5_35
BANK13_LVDS_0_P/N	87,89	R17/T17	**AA14/AA15**	**IO_L11_SRCC_13**
BANK13_LVDS_1_P/N	88,90	U19/V19	**Y14/Y15**	**IO_L12_MRCC_13**
BANK13_LVDS_2_P/N	91,93	Y18/Y19	U19/V19	IO_L20_T3_13
JX2 (Bank 34 and some Bank 13)				
JX2_LVDS_0_P/N	17,19	T2/T1	M4/M3	IO_L22_T3_34
JX2_LVDS_4_P/N	29,31	U2/U1	P7/R7	IO_L24_T3_34
JX2_LVDS_7_P/N	36,38	K4/K3	P3/P2	IO_L18_T2_34
JX2_LVDS_10_P/N	47,49	M4/M3	**K4/K3**	**IO_L11_SRCC_34**
JX2_LVDS_11_P/N	48,50	P7/R7	**L5/L4**	**IO_L12_MRCC_34**
JX2_LVDS_12_P/N	53,55	L5/L4	**T2/T1**	**IO_L13_MRCC_34**
JX2_LVDS_13_P/N	54,56	P3/P2	**U2/U1**	**IO_L14_SRCC_34**
JX3 (Additional Bank 13)				
BANK13_LVDS_7_P/N	73,75	AA11/AB11	**Y18/Y19**	**IO_L13_MRCC_13**
BANK13_LVDS_8_P/N	74,76	U11/U12	**AA16/AA17**	**IO_L14_SRCC_13**
BANK13_LVDS_9_P/N	79,81	V11/W11	AA11/AB11	IO_L7_T1_13
BANK13_LVDS_11_P/N	85,87	AA12/AB12	V11/W11	IO_L4_T0_13
BANK13_LVDS_14_P/N	92,94	V15/W15	R17/T17	IO_L19_T3_13
BANK13_LVDS_15_P/N	97,99	Y14/Y15	V15/W15	IO_L2_T0_13