PicoZed FMC Carrier Card
Revision C
Errata

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2 Introduction

Thank you for your interest in the PicoZed FMC Carrier Card (PZCC-FMC). Although Avnet has made every effort to ensure the highest possible quality, these boards are subject to the limitations described in this errata notification. This document pertains to the PicoZed FMC Carrier Card Revision C.

Please be aware that any of the optional workarounds requiring physical modifications to the board are done at the User's own risk. Avnet is not liable for poorly performed rework.

3 Identifying Affected Boards

The Revision C PicoZed Carrier boards affected by these errata can be identified by the Revision of the PicoZed Carrier in the kit. The Revision of the PicoZed Carrier can be found on the backside inlay MBCC-PZCC-PCB-C as shown below:

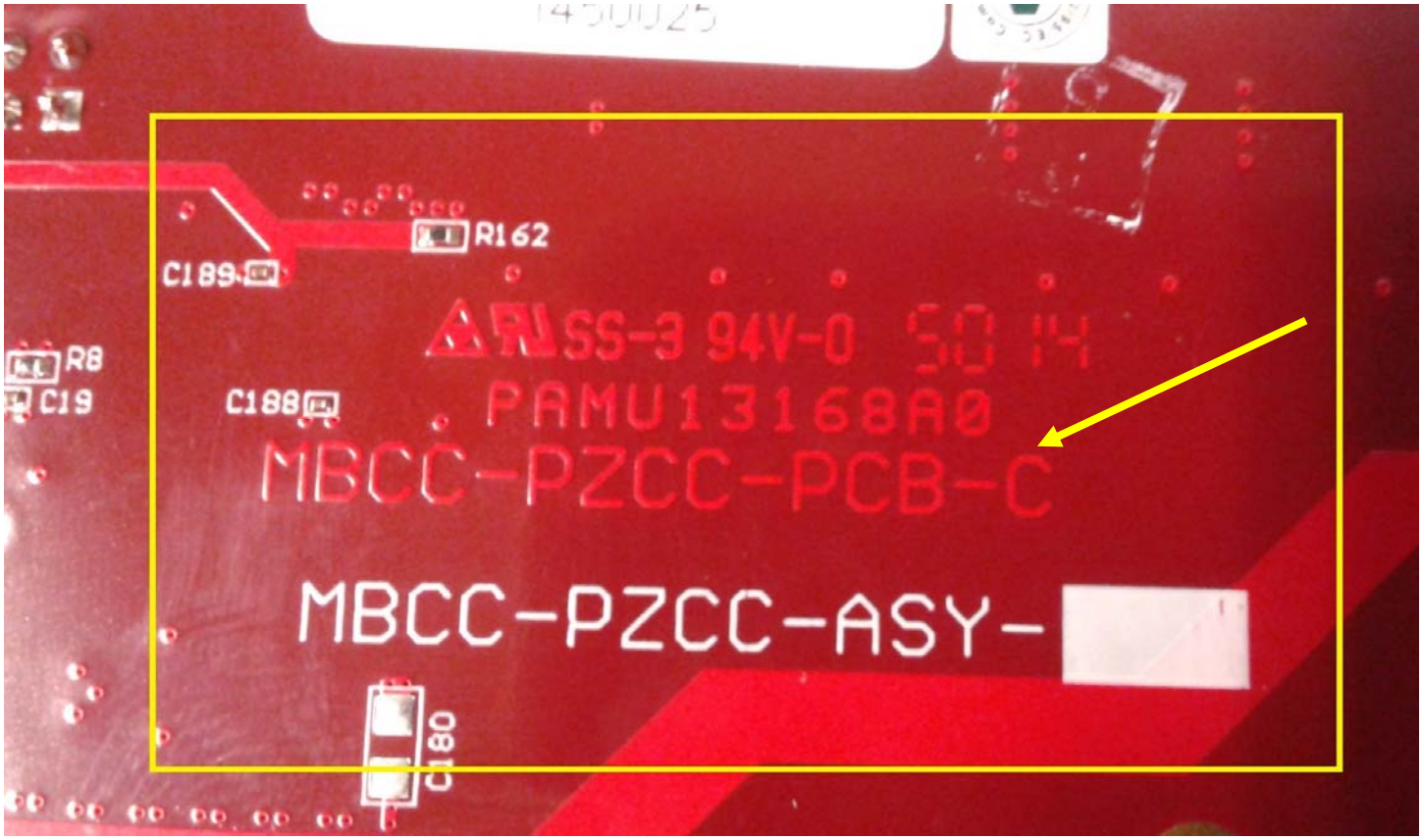

Figure 1 – Identifying PicoZed Carrier Board Revision

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4 Errata

4.1 Ethernet Address conflict on SOM and Carrier Card

Applications Affected

Revision C builds prior to April 1st, 2015 and earlier PZCC-FMC boards. There are no known field failures due to this issue. However, it is possible with future releases of the Xilinx GMII-to-RGMII shim in the PL that a failure may result.

Description

The secondary Marvell 88E1512 PHY on PicoZed FMC Carrier sets the PHY's MDIO address to 0, which is the MDIO broadcast address. Since the Xilinx GMII-to-RGMII shim is also on the MDIO bus, the shim could potentially interfere with communication to the PHY (although the shim does not respond to the broadcast address as of Vivado 2014.4).

Workaround

Remove R80. Wire the top of R146 to the right pad of R80. This changes the PHYAD[0] from a '0' to a '1'.

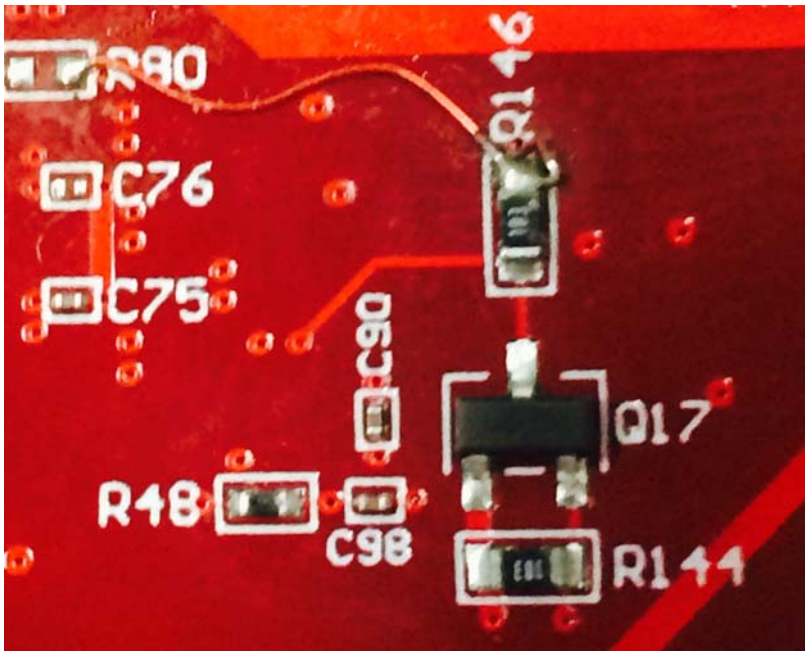

Figure 2 – Rework which changes Ethernet Port J11 to Address 0x01

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4.2 Ethernet RGMII on Bank 13 at 3.3 volts

Applications Affected
There are no known field failures due to this issue.

Description
The PZCC-FMC's Ethernet PHY currently connects to Zynq Bank 13 on the SOM, with VCCO_13 = 3.3V. According to Xilinx PG160, an RGMII interface at 3.3V is not supported. However, the Marvell PHY clearly supports 3.3V. Avnet has not been notified or experienced any testing or customer issues, including failures, with the current power method.

Workaround
There are no workarounds at this time.

4.3 Ethernet Reset delay

Applications Affected
There are no known field failures due to this issue.

Description
Per Marvell, the PZCC-FMC's Ethernet PHY RESET_N pin needs to be held low for a minimum of 10mS during power up.

Workaround
Hold or assert a low on JX3.66 PS_ETHRST_N l for 10mS after the SOM power stabilizes. Alternatively, a resistor and capacitor with a minimum 3 tau time constant (such as 10K and 0.47uF) exceeding 10mS can be added to the output of U16.4.

4.4 Ethernet Oscillator U10 phase jitter

Applications Affected
There are no known field failures due to this issue.

Description
The current 25 MHz oscillator connected to the PZCC-FMC's Marvell 88E1512 PHY does not meet Marvell's jitter specification. Marvell recommends a lower phase jitter part (1ps or less).

Workaround
Replace the U10 oscillator with a lower phase jitter variant. The recommended Abracon part number is: ASD3-25.000MHZ-LR-T/BKN.

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4.5 Ethernet RX_CLK not connected to Clock Capable pin

Applications Affected
An Ethernet circuit using the PZCC-FMC's Ethernet PHY and a PL-based MAC will not build properly.

Description
The Marvell PHY ETH_RX_CLK pin, U9.46 (JX2.94) is not routed to a SOM clock capable pin. When attempting to use a PL-based MAC connected to this PHY, the tools will generate an error since this clock needs to be connected to a Zynq clock-capable pin for the clock routing inside the PL to work properly.

Workaround
The easiest workaround is to use the PS GEM1 routed through EMIO to this PHY. The PS GEM does not have the same requirements for the RX_CLK to be connected to a clock-capable pin.

If a PL-based MAC is required, it may be possible to rewire the Rev C board to accomplish this. This rework has not been performed or verified by Avnet. The user can swap JX2.94 (ETH_RX_CLK) signal to JX3.74 (PMOD1_D0_P) via hardware board rework.

4.6 FMC +3.3V current draw

Applications Affected
PicoZed Carrier Card Revision C or earlier with a PicoZed SOM and a FMC card requiring 3 amps on the 3.3V Rail.

Description
The LPC-FMC specification indicates the 3.3V rail should be capable of sourcing 3.0 amps. The inductor, L16, on the PZCC is rated at 3.0 amps thereby leaving no significant current available for the SOM's bank VCCO_13 or other Carrier circuitry connected to 3.3V. This condition may cause system instability if a FMC board needs maximum current on 3.3V.

Workaround
Replace L16 with a higher current footprint compatible inductor. The recommended part number is Bourns SRU6025-1R2Y which is a 4 ampere part. The C03 boards have the new inductor installed, so there is no action required by the user.

4.7 FMC differential pair pinout

Applications Affected
FMC boards attached to the PicoZed Carrier Card using lower ordered FMC pairs.

Description
The FMC differential pairs are routed across all three JX connectors and FPGA banks. At minimum, the lowest 16 FMC pairs should be routed to one connector and FPGA bank to allow maximum FMC flexibility.

Workaround
Due to the complexity, cost and risk of the rework required, Avnet has not performed this re-work on production boards.

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4.8 Impedance resistors on FMC Clocks

Applications Affected

FMC module applications utilizing any of the three clocks from FMC to Zynq: GBTCLK0_M2C, CLK0_M2C, or CLK0_C2M.

Description

Impedance matching resistors R23, R24 and R25 were placed to ensure impedance matching to a FMC module. However, these resistors may be removed because the SOM FPGA fabric has internal matching resistors that can be used. To improve signal integrity it is recommended these components be removed and the SOMs FPGA fabric configured appropriately.

Workaround

In Revision C03, Avnet removed resistors R23, R24, and R25. The user needs to terminate in the SOM's FPGA fabric.

4.9 1.8V HDMI and Ethernet rail

Applications Affected

Applications that use the HDMI and the carrier's U9 88E1512 Ethernet interface simultaneously.

Description

The 1.8V rail is limited to 200mA by U11. During HDMI and simultaneous PHY (U9) activity one or both of these interfaces may become unstable and operate erratically or not at all.

Workaround

There are no known workarounds other than to use one interface at a time.

4.10 Vadj rail current limits

Applications Affected

FMC and/or bank 34 and 35 applications approaching the FMC Vadj 2.0 amp limit per the Vita 57 specification.

Description

Per the ADP5052 Revision 0 datasheet, Channel 3, the Vadj rail can source 1.2 amps. Testing has yielded a minimum capability of 1.6 amps which is also listed further in the datasheet. However, in keeping with the FMC specification, it should be noted that FMC boards and/or bank 34 and 35 applications that exceed the 1.2 Amp limit may experience anomalous behavior.

Workaround

There are no known workarounds at this time.

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4.11 PL Pmod Level Translators

Applications Affected

PL Pmods in a differential configuration or when VADJ is set to 2.5V or 1.8V.

Description

The PL Pmod connections (J3 and J4) have voltage level translators to translate between 3.3V and Vadj. However, the PL Pmod I/Os are connected to Bank 13, which has VCCO connected to 3.3V, making these level translators unnecessary. Setting VADJ to 2.5V or 1.8V may introduce data errors. Furthermore, these translators do not allow differential signaling to the Pmod interfaces.

Workaround

When the PicoZed 7010, 7015, or 7020 SOMs are attached, VADJ may be set to 3.3V for the Pmods to work properly in low-speed, single-ended mode.

The PicoZed 7030 requires that VADJ be set to 1.8V or the SOM will be damaged. In this situation, a potential workaround to enable low-speed, single-ended mode is:

1. Lift U17.Pin2 and rewire to 3.3V
2. Desolder R162 off the VADJ pad and tie to 3.3V instead
3. Lift U17.Pin2 and rewire to 3.3V
4. Desolder R162 off the VADJ pad and tie to 3.3V instead

There is no simple workaround to allow differential signaling on the Pmods. However, the customer may pursue a solution by removing Q1, U2, U4, U17, and U18 and wire across the removed IC pads. It is expected that this would work for all PicoZed SOM types. Due to the complexity and cost of the rework required and the possibility of putting SFP+ data on a Pmod interface, Avnet has not performed this work around.

4.12 PCIe Jitter Attenuator signal integrity components

Applications Affected

PicoZed Carrier Card Revision C or earlier attached to a PicoZed SOM while inserted into a PCIe slot.

Description

DC blocking capacitors were placed at locations C151 and C152 to provide DC isolation to the SOMs. R169 was placed to ensure impedance matching. However U13 has an internal impedance of 100 ohms and the SOMs have these blocking capacitors already placed. To improve signal integrity it is recommended these components be removed. C151 and C152 must be replaced with a zero ohm resistor.

Workaround

In Revision C03, Avnet replaced C151 and C152 with a zero ohm resistor such as P/N: CRCW02010000Z0ED.
Remove R169.

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4.13 MGT Clock Multiplexer signal integrity components

Applications Affected

PicoZed Carrier Card Revision C or earlier attached to a PicoZed SOM while using the transceiver on an FMC card.

Description

DC blocking capacitors were placed at locations C153, C154, C181 and C182. However, per the FMC specification ANSI/VITA 57.1-2008 (R2010), FPGA Mezzanine Card (FMC) Standard, no carrier card components should be placed on these signals. If components are necessary, the FMC module is to contain the necessary components. To improve signal integrity, it is recommended these components be removed and replaced with zero ohm resistors.

Workaround

In Revision C03, Avnet removed C153, C154, C181 and C182 and replaced with zero ohm resistors such as P/N: CRCW02010000Z0ED.

4.14 SFP+ P2 connector change

Applications Affected

PicoZed Carrier Card Revision C or earlier attached to a PicoZed 7015/7030 SOM while using a SFP+ module.

Description

The SFP+ connector, P2, was not populated with a SFP+ capable plug. This could potentially lead to lower SFP data rates.

Workaround

In Revision C03, Avnet replaced P2 with an SFP+ connector PN: 1888247-1.

4.15 SFP+ TX Data Rate select signal

Applications Affected

Application using the PicoZed 7015/30 SOM with an SFP+ module.

Description

P2 pin 9 is labeled as VeeR and is connected to ground. This pin should be labeled RS1 (TX Rate Select 1) and attached to a JT jumper or FPGA GPIO pin to allow data rate selection of Low Bandwidth or High Bandwidth. With this pin is attached to ground, the data rate is set to Low Bandwidth – 2.125 Gb/s or 4.225 Gb/s.

Workaround

Due to the complexity, cost and the possibility of damaging the SFP+ area with this rework, Avnet has not performed this re-work on C03 production boards. To select a High Bandwidth data rate (8.5 Gb/s), the customer can remove the SFP+ cage and cut the P2.10 trace. Attach pin P2.10 to 3.3V via a 1K ohm pullup resistor.

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4.16 SFP+ signal integrity components

Applications Affected

PicoZed Carrier Card Revision C or earlier using the PicoZed 7015/30 SOM in an SFP+ application.

Description

DC blocking capacitors were placed at locations C162 and C163. However, SFP+ modules have these parts placed if necessary. To improve signal integrity it is recommended these components be removed and replaced with zero ohm resistors.

Workaround

In Revision C03, Avnet removed C162 and C163 and replaced with zero ohm resistors such as P/N: CRCW02010000Z0ED.

4.17 SMA max link speed

Applications Affected

PicoZed Carrier Card with PicoZed SOM attached using the SMA interfaces.

Description

The maximum PRBS31 SMA link speed with zero errors is 3.75 Gb/s using IBERT in Vivado 2015.1. Reducing the PRBS number results in higher link speeds. 6.25 Gb/s has been measured on the SMAs using PRBS7.

Workaround

There are no known workarounds to achieve a higher PRBS31 data rate.

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4.18 J13 Power Test

Applications Affected
Power testing the PicoZed Carrier Card without a SOM using J13.

Description
J13, when placed, cannot start up the carrier's power supply as intended. This is because 3.3V is not available on the board (because the power supply is not turned on).

Workaround
Due to the complexity and cost of the rework, Avnet did not implement any changes on the C03 board. However, the customer can still perform power supply measurements by attaching a programmed SOM onto the carrier and powering the carrier on. CON3 can then be used to measure power supply voltages.

If the customer chooses to test the power supplies on the carrier board without a SOM, the following rework can be performed.

Temporary test method:
Apply a 1.8V, 10mA current limited signal to J13 pin 2 (the left side of the connector when viewed from above).

Permanent test method:
Create a 1.8V divider on the board using resistors. Remove R104. Attach a resistor divider to C96 (+5V, VIN_HDR). Top resistor (3.24K) goes to C96, bottom resistor (1.78K) goes to ground. Attach a wire from the center tap of the resistive divider to J13.1. This provides a 1.77V output. Place a jumper on J13 to enable the on board power supplies without a SOM placed.

4.19 J5 and J6 MicroUSB headers

Applications Affected
PicoZed Carrier Card Revision C or earlier attached to USB interfaces.

Description
The prior J5 and J6 connectors had the potential to shear off if too much lateral force was applied.

Workaround
In Revision C03, Avnet replaced J5 and J6 with new PN: 475890001 which has two vertical pins soldered into the PCB to alleviate potential shear issues.

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4.20 USB UART Enumeration

Applications Affected

PicoZed Carrier Card attached to the USB-UART interface.

Description

The USB UART CP2104 VIO pin back-feeds the 3.3V rail causing intermittent UART enumeration when the PZCC board is turned off. To ensure consistent enumeration, the VIO pin is required to be connected to the CP2104's VDD pin. To ensure proper reset sequence, the RST_N pin should also be tied to the VDD pin.

Workaround

Power sequence method:

Plug in the Carrier Card and power on. Plug in the microUSB to the USB UART port. As long as the USB-UART is connected, the board can be power cycled or reset without requiring further USB enumeration.

Hardware rework method:

Due to the complexity, cost and the possibility of damaging the UART area with this rework, Avnet has not performed this re-work on C03 production boards. The customer can pursue a solution by cutting the 3.3V trace to U5.5 (VIO) and attaching the pin to U5.6 (VDD). For the RST_N rework, the 3.3V trace to R20 can be cut. This end of R20 can then be attached to U5.6 (VDD).

4.21 USB Host Vbus Current Is Low

Applications Affected

PicoZed Carrier Card with the USB 2.0 port configured as USB Host. A USB device requiring power plugged into J5 may not receive enough power.

Description

When the PicoZed FMC Carrier is configured for the USB 2.0 to be in Host mode, 500 mA should be available on Vbus for a device plugged in. Unfortunately, this is not the case for the PicoZed FMC Carrier. A NC7SZ66 bus switch (U15) is used in to deliver power to Vbus in Host mode which is only rated at 128mA. USB Devices may not enumerate properly when plugged in due to insufficient power.

Workaround

A work-around for this is to use a powered USB hub plugged into the PicoZed FMC Carrier USB 2.0 Host port (J15).

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4.22 SMA Connectors are of the incorrect style

Applications Affected

PicoZed Carrier Card with a serial number within the range of 1450530-1450629 where customer is trying to use the SMA connectors of the board.

Description

Located at position J15, J16, J19, J20, J21, J22, you will notice that instead of SMA connectors SMB style has been installed. While measures are in place to minimize manufacturing defects, there exists the possibility of the wrong part being placed. In this case, the SMA connector called out in the bill of material has not been placed.

Figure 3 – SMB Connector vs SMA Connector

Workaround

If your FMC Carrier Card falls within the affected serial number range and has the SMB connectors populated you have the following options:

- If you are not working with the transceivers, these connectors are not used, no action required
- Use the connectors as-is with an SMB cable.
- Return the board to Avnet for connector replacement.

If support is needed contact your local Silica or Avnet FAE, or your local sales office.

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NOTES - PLEASE READ:

1. **When booted from the factory QSPI image, the PicoZed 7015/30 boards manufactured prior to June 12, 2015 do not boot past the U-Boot prompt and therefore do not configure the PL (the blue DONE LED will not light) nor does it boot into the PetaLinux load on the eMMC. This is not a PZ or PZCC hardware issue, but rather a software glitch in the tools that is being resolved by Avnet. The new images will be programmed into the new PicoZeds when available. Customer's with the current 7015/30 SOM can update their programmed images from the archive provided on the .org site (**http://picozed.org/content/picozed-flash-upgrade)

   This is no way affects the quality of the boards, as they had to complete a full functional test before leaving the factory. You can verify that your board is in expected condition by checking the output on the USB-UART terminal:

```
U-Boot 2014.01-dirty (Sep 29 2014 - 09:07:05)

I2C:   ready
Memory: ECC disabled
DRAM:  1 GiB
MMC:   zynq_sdhci: 0, zynq_sdhci: 1
Using default environment

In:    serial
Out:   serial
Err:   serial
Net:   Gem.e000b000
Hit any key to stop autoboot:  0
Copying Linux from QSPI flash to RAM...
Unknown command 'sf' - try 'help'
zynq-uboot>
```

   Boards affected by this issue will have a Serial Number less than or equal to the numbers below:

   BD-Z7PZP-7Z015-G REV C01
   Serial 1415249

   BD-Z7PZP-7Z030-G REV C01
   Serial 1412248

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5 New Erratum

Any new erratum found will first be posted in the PicoZed Forums:
http://picozed.org/forums/picozed-hardware-design

Since this document will only be updated periodically, it is recommended that the PicoZed Forum also be checked for other, recently found erratum.

6 Additional Support

For additional support, please review the discussions and post your questions to the PicoZed Forum at http://picozed.org/forums/picozed-hardware-design .

You can also contact your local Avnet/Silica FAE.

7 Revision History

Date	Version	Revision
08 APR 2015	1.0	Initial Version, PicoZed FMC Carrier Revisions B & C.
12 JUN 2015	1.1	Updated revision including silicon MFGs feedback.
07 OCT 2015	1.2	Added item 4.21 regarding USB Host 2.0 current limit. Added serial numbers of affected units in Notes.
15 NOV 2016	1.3	Added section 4.22 regarding SMA Connector issue

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